Enabling the Expanding Cloud: High-Bandwidth Memory and 2.5D Solutions

eSilicon Corp.

TSMC 2016
Open Innovation Platform®
Ecosystem Forum

ABSTRACT

The next generation of high-performance computing, graphics and networking applications have increasing needs for bandwidth. If we look at a traditional ASIC with external memory, the complete system is large with many DRAMs taking up board real estate affecting the performance and power consumption. The performance suffers from increased latency of the signals and more power results from driving these signals. In addition to this, there is a significant growth of the number of tracks on the substrate as well as an increase in the number of die leading to routing congestion.

DRAM technology has not been scaling to keep up with this need. The answer is moving to a stacked memory solution – high-bandwidth memory (HBM). This memory has been defined as a JEDEC standard, JESD235A, and began production in 2015. The use of HBM requires 2.5D packaging with silicon interposer and through-silicon vias.

2.5D technology offers a tremendous increase in capacity and performance. Increased capacity because of the stacked memory in a smaller area and increased performance because of the interposer and shorter signal routing. The interposer allows the integration of highly parallel connections to the memory stacks inside the package, therefore it is able to offer huge capacity and performance increases.

eSilicon started a program called “Modular Z-axis Integration” or MoZAIC in 2011. As an ASIC provider of large, complex networking and communication systems, we began analyzing new approaches that would provide more bandwidth for our customers. This includes the development of an HBM PHY in 28nm and FinFET technologies as well as the study of 2.5D packaging. eSilicon has completed seven test chips to date that verify the HBM PHY IP and to vet the supply chain in support of 2.5D integration — design, verification, test and reliability.

This presentation will highlight the silicon characteristics of eSilicon’s HBM PHY in TSMC’s CLN28HPC technology. The presentation will also highlight TSMC CoWoS technology as well as complex ASICs that use high-bandwidth memory.

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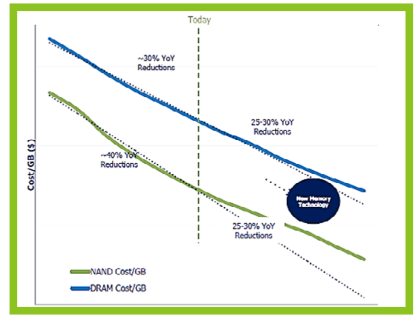
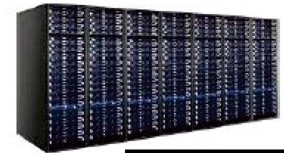
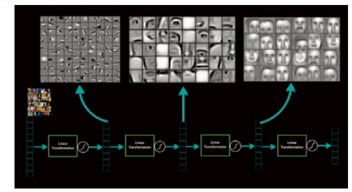
Lisa Minwell
SR. DIRECTOR IP MARKETING

What's Driving High Bandwidth Memory?



Source: Mike Black, Micron, EDPS 2013

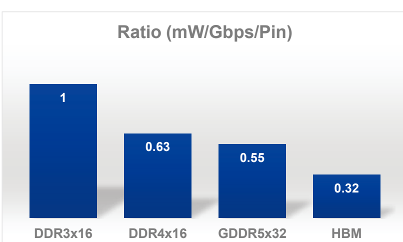


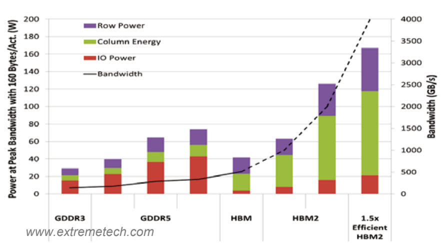


- DRAM technology in sub-20nm technologies faces severe challenges, such as difficulties in obtaining sufficient storage capacitance and sensing margin leading to stacked memory
- The need for increased bandwidth is driven by the growing IoT cloud, deep learning and neural networks

The Power Problem

- Limited bandwidth of DDRx devices now requires very high numbers of DRAM devices connected to the central ASIC
  - To buffer 1Tbps would require 40 DDR3 DRAMs all connected through separate buses
- ASICs are already at >1,500 pins and typically pin-limited. Very difficult to increase bandwidth to memory using current approach
- DDR4 does not solve the problem – 1Tbps requires 20 DDR4 DRAMs





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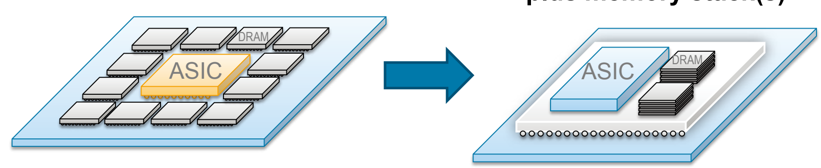
2.5D Increases Bandwidth

ASIC plus multiple DRAMs

Single package - ASIC plus memory stack(s)



- Using an interposer allows the integration of highly parallel connections to memory stacks inside the package
- Much higher total bandwidth
- Significant reduction in power consumption
- Much smaller board footprint

2.5D and HBM DRAM Architecture

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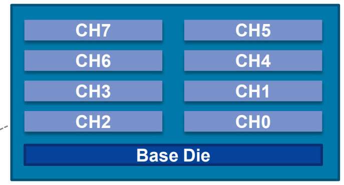
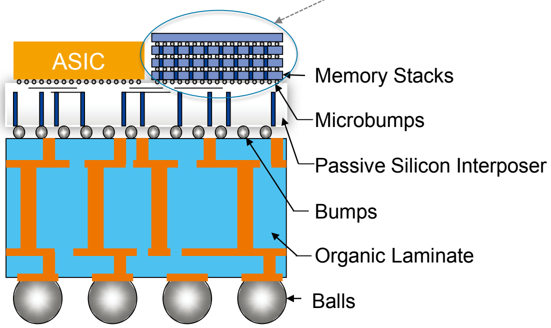
- High-Bandwidth Memory Stack
  - Base die – JTAG, BIST, PHY, through-silicon via (TSV) and DA interfaces
  - Core die – (CH0 – CH7) DRAM circuitry and TSV interface



HBM Four-High Stack



HBM Implementation Has Its Challenges

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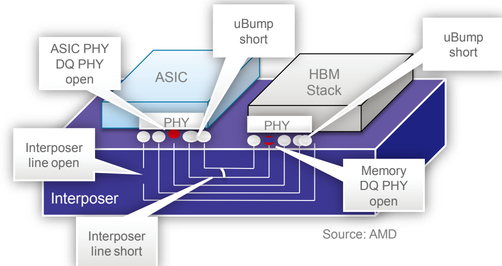

Challenges:

8192-bit-wide memory bus is, by conventional standards, absurdly wide, requiring thousands of contacts and traces

The key challenge is that the max junction temp acceptable for the HBM2 die is a lot lower than the ASIC while at the same time the thermal coupling to the high-power ASIC is significant.

Solutions:

- Repair interconnection failure between SoC and HBM using MISR test to validate connections
- Redundant uBumps used for AWORD/DWORD repair
- Careful thermal and power analysis for the entire module in the design phase and additional thermal test vehicles to validate thermal and reliability assumptions

HBM Implementation Recipe

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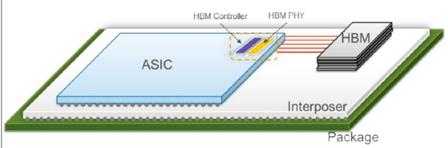
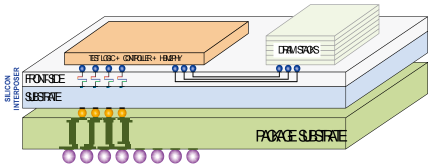
Design & Implementation



Characterization, Reliability & Test



HBM PHY & Controller	• Hardened for optimal speed and integration • Supports multiple HBM vendors for expanded supply chain
Interposer Design	• Single and power integrity • Thermal and warpage analysis
Characterization	• Fully tested to meet performance
Reliability & Testability	• Package test • Assembly stacking • HTS, pre-conditioning,TC and unbiased HAST
Wide Supply Chain	• Lowest cost • Fastest time to market

Proving the Supply Chain FinFET Logic Die and Silicon Interposer

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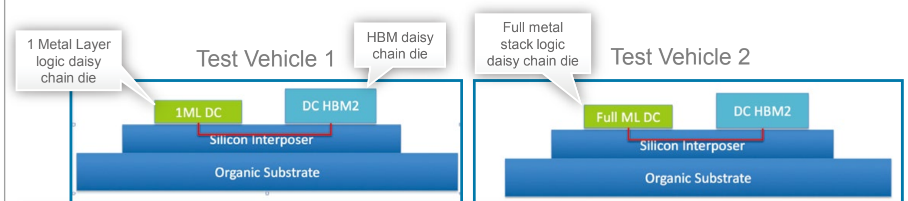
Incremental test vehicles enable customers to meet tight schedule deadlines while implementing this new technology

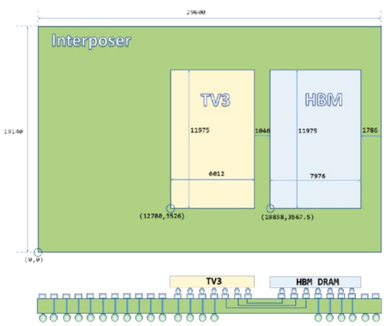


	Test Vehicle 1		Test Vehicle 2
Interposer Design Process Validation	✓	1LM	Full ML ✓
Assembly Stacking Validation	✓	Adjustments	✓
BOM Validation	✓	Adjustments	✓
Package Test (HTS, preconditioning, TC & unbiased HAST)	Level 1		Level 2

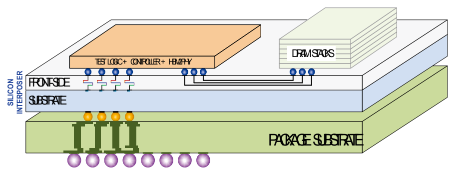
EDA Track
IP Track
EDA / IP / Services Track
Print-Only Papers

HBM PHY Test System Interposer – Test Vehicle 3

eSilicon leverages both ASIC and IP design



- Thermal test vehicle combined with the IP qualification vehicle (TV3)
- PHY development and test
- Interposer design
- Packaging
- Warpage analysis

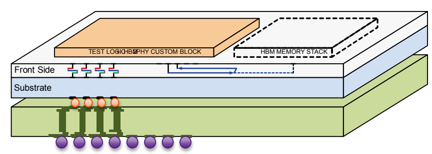


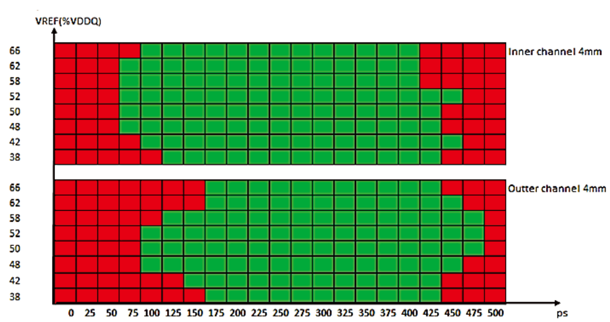
eSilicon's HBM IP Manufacturing Tests

Test	ASIC Wafer	ASIC Die & Interposer & Package	Package; Includes HBM2	Notes
PLL Test	X	X	X	
DLL BIST	X	X	X	Validate every DLL delay line tap
HBM Internal Loopback	X	X	X	Through driver, to-pad
SerDes Internal Loopback	X	X	X	
SerDes External Loopback		X	X	
HBM Memory Soft Repair			X	Hard repair done in memory manufacturing test
PMBIST ASIC DRAM Test			X	Soft programmable
ASIC/HBM MISR AC Test			X	LFSR/MISR through IEEE-1500 interface
uBump Soft Repair			X	Based on MISR test results
HBM DC Boundary Scan			X	IEEE-1500 based – post MISR/repair
PVT Sensors	X	X	X	Through-tap controller. Burn at wafer if trimming needed
ChipID/eFuse	X	X	X	Through-tap controller. Burn at wafer
Functional Vectors	X	X	X	For scan AU fault detection

eSilicon's CLN28HPC HBM Gen2 PHY Silicon Results

November 2015 TSMC CyberShuttle with interposer CoWoS

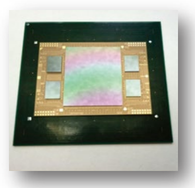




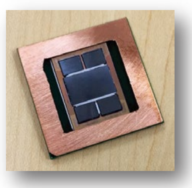
2D eye diagram for TT, 1.2V/0.9V and 25C (~4mm interposer route)

eSilicon HBM Customer Programs

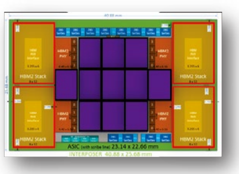
Organic Interposer
ASIC with four HBM1 stacks

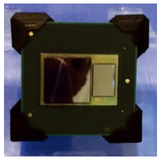


28nm
ASIC with four HBM1 stacks

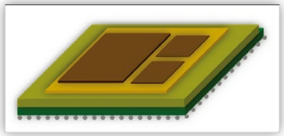


28nm
ASIC with four HBM2 stacks

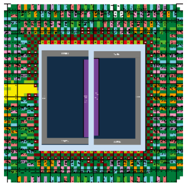




FinFET
ASIC with one HBM2 stack

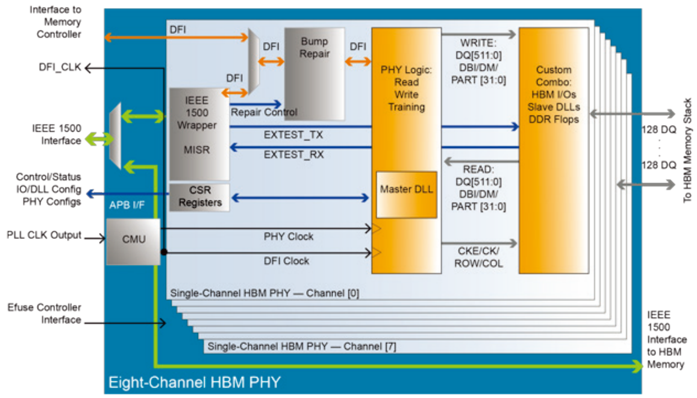


FinFET
ASIC with two HBM2 stacks



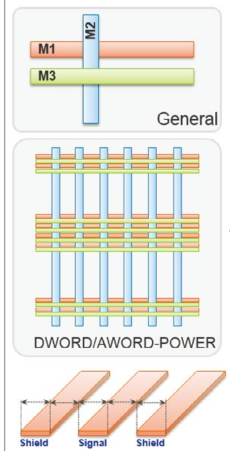
FinFET
Two ASIC dies implementing chip-to-chip communication

eSilicon HBM PHY IP

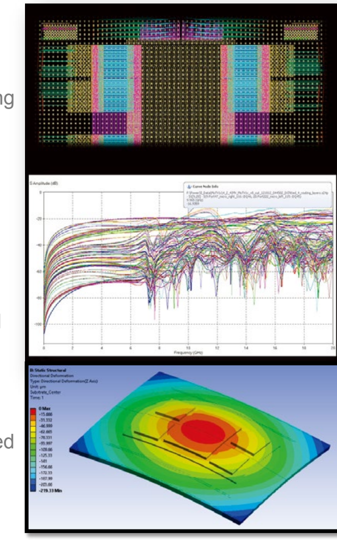


- All high-speed circuits are implemented with hand-crafted layout
- DFI and APB interfaces
- IEEE1500 and eFuse controller interfaces
  - PHY test modes, ubump repair, trimming

eSilicon 2.5D Services



- **2.5D interposer and package design**
  - Interposer and package routing
  - Design for manufacturability (DFM)
  - SI/PI design and analysis
  - Thermal integrity
  - Warpage analysis
- **Single production source for:**
  - Acquisition / assignment of all die in package
  - Assembly
  - Test
  - Delivery of final, tested, yielded devices

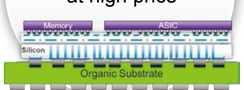


Interposer Technology Adoption

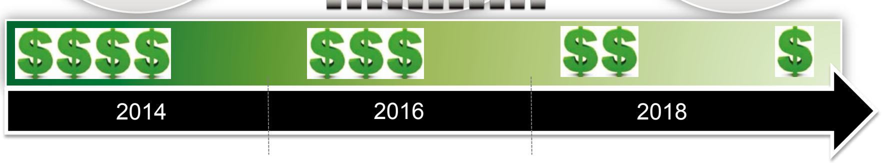
CoWoS

Trend #1
Extend the lifetime of existing packaging technologies

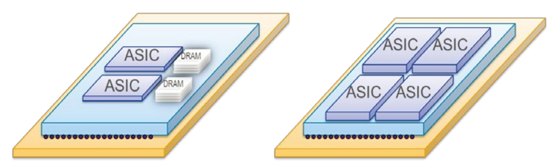
Trend #2
2.5D adoption for high-end markets at high price

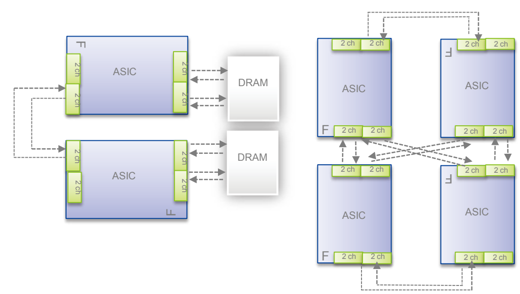


Trend #3
2.5D: Lower cost with build-up or organic interposers and use of FOWLP for additional connection density



New Programs Combining HBM and Chip-to-Chip





Combo PHY to support both HBM and chip-to-chip communication

What's Needed for the Optimal HBM Implementation?

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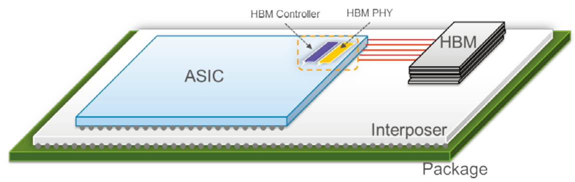
Achieving high-bandwidth and low-power benefits with a low-cost, low-risk, complete solution



- Controller & PHY Integration
- Characterized Performance
- Interposer Design
- Wide Supply Chain
- Reliability & Test

eSilicon and TSMC have the solution

tsmc

eSilicon®

The right chip. Right now™